II. Listing of Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) An advanced process control (APC) method for an oxide, metal, or barrier layer polish process in a polish tool that minimizes within wafer and wafer to wafer sheet resistance (Rs) variations in a plurality of wafers having a metal layer formed on a barrier layer within an opening in a dielectric layer, said metal layer has a thickness, width, and cross-sectional area, comprising:

(a) providing a plurality of wafers each having a metal layer that has been formed on a barrier layer within an opening in a dielectric layer by a sequence of processing steps; said processing steps include at least one patterning step, CVD step, etch step, and metal deposition step;

(b) determining a relationship between the cross-sectional area of said metal layer and Rs;

(c) determining a total Rs (Rs_{TOTAL}) for the metal layer on each of said plurality of wafers before said oxide, metal, or barrier layer polish process;

(d) determining an oxide, metal, or barrier layer polish thickness target for said metal layer on each of said plurality of wafers; and

(e) calculating an oxide, metal, or barrier layer polish time for each of said plurality of wafers in the oxide, metal, or barrier layer polish process.

2. (Original) The method of claim 1 wherein said metal layer is comprised of copper and the barrier layer is comprised of TaN and said oxide, metal, or barrier layer polish process is performed in a CMP tool that polishes one or more of said copper layer, TaN barrier layer, and dielectric layer simultaneously.

3. (Original) The method of claim 1 wherein the relationship between the cross-sectional area of said metal layer and Rs is determined by plotting (1/cross-sectional area) vs. Rs results for a plurality of wafers and line fitting the data.

4. (Original) The method of claim 1 wherein the total Rs is determined from the equation:

$$Rs_{TOTAL} = Rs_{PHOTO} + Rs_{CVD} + Rs_{ECP} + Rs_{ETCHING}$$

where Rs_{PHOTO}, Rs_{CVD}, Rs_{ECP}, and $Rs_{ETCHING}$ are terms that represent contributions from a patterning (photo) step, a CVD step, a metal deposition (ECP) step, and an etching step, respectively, to a variation in the width and thickness of said metal layer.

5. (Original) The method of claim 1 wherein said oxide, metal, or barrier layer polish thickness target for said metal layer is determined from the relationship in step (b), the Rs_{TOTAL}, and the desired Rs value (Rs target value) for said metal layer in each of the plurality of wafers.

6. (Original) The method of claim 1 wherein the oxide, metal, or barrier layer polish time is determined by using the equation:

$$PT_t = Rs_T - Rs_{TOTAL} / \alpha$$

where PT_t is the polish time for a particular wafer, Rs_T is the Rs target value provided for said metal layer, α is the polish rate in said oxide, metal, or barrier layer polish process, and Rs_{TOTAL} is the value from step (c).

7. (Original) The method of claim 6 further comprised of modifying the polish time in step (e) based on post oxide, metal, or barrier layer polish measurement data by including a disturbance factor (d_K) wherein the modified equation is the following:

$$PT_t = Rs_T - Rs_{TOTAL} / \alpha + d_K$$

where $d_K = (1 - \lambda)d_{K-1} + \lambda\ (Rs_T - Rs_{n,\ TOTAL} - \alpha\ PT_{K-1})$ in which d_{K-1} and PT_{K-1} indicate a disturbance factor and oxide, metal, or barrier layer polish time, respectively, for the (n-1)th wafer in the plurality of wafers, $Rs_{n,\ TOTAL}$ is Rs_{TOTAL} for the nth wafer in a plurality of wafers, and λ is a numerical value between 0 and 1.

8. (Original) The method of claim 7 wherein d_{K-1} is equal to 0 for the first wafer in the plurality of wafers to be oxide, metal, or barrier layer polished.

9. (Original) The method of claim 7 wherein said post oxide, metal, or barrier layer polish measurement data includes the polish rate of said metal layer in said oxide, metal, or barrier layer polish step on at least one wafer that has been processed in the process tool.

10. (Original) The method of claim 7 wherein any filter algorithm may be used to update said d_{K-1}.

11. (Original) The method of claim 1 wherein said steps (b) – (e) are performed by a computer that is part of an advanced process control (APC) system which includes an APC controller that receives input from the computer and sends commands to one or more polish tools via a tool application program (TAP) and tool control system (TCS).

12. (Original) The method of claim 11 wherein the computer contains a feed forward (FF) model and a feed backward (FB) model wherein the FF model receives measurement data related to said sequence of processing steps and is used to perform steps (c) – (e) and wherein the FB model receives post oxide, metal, or barrier layer polish measurement data and is also used for step (e).

13. (Original) An APC method for an oxide (Cu, or TaN) polish step in a CMP tool that minimizes within wafer and wafer to wafer sheet resistance (Rs) variations in a plurality of wafers having a copper layer, said copper layer has a thickness, width, and cross-sectional area and is formed on a TaN layer in an opening within a dielectric layer, comprising:

(a) providing a plurality of wafers each having a copper layer that has been formed on a TaN layer in an opening within a dielectric layer by a sequence of processing steps; said processing steps include at least one patterning step, CVD step, etch step, and copper deposition step;

(b) determining a relationship between the cross-sectional area of said copper layer and Rs;

(c) determining a total Rs for the copper layer on each of said plurality of wafers before said oxide (Cu, or TaN) polish process;

(d) determining an oxide (Cu, or TaN) polish thickness target for said copper layer on each of said plurality of wafers; and

(e) calculating an oxide (Cu, or TaN) polish time for each of said plurality of wafers in the oxide (Cu, or TaN) polish process.

14. (Original) The method of claim 13 wherein said oxide (Cu, or TaN) polish process reduces the thickness of one or more of said copper layer, TaN layer, and dielectric layer.

15. (Original) The method of claim 13 wherein said opening is a trench or a trench formed above a via.

16. (Original) The method of claim 13 wherein the relationship between the cross-sectional area of said copper layer and Rs is determined by plotting (1/cross-sectional area) vs. Rs results for a plurality of wafers and line fitting the data.

17. (Original) The method of claim 13 wherein the total Rs is determined from the equation:

$$Rs_{TOTAL} = Rs_{PHOTO} + Rs_{CVD} + Rs_{ECP} + Rs_{ETCHING}$$

where Rs_{PHOTO} , Rs_{CVD} , Rs_{ECP} , and $Rs_{ETCHING}$ are terms that represent contributions from a patterning (photo) step, a CVD step, a copper deposition (ECP) step, and an etching step, respectively, to a variation in the width and thickness of said copper layer.

18. (Original) The method of claim 13 wherein said oxide (Cu, or TaN) polish thickness target for said copper layer is determined from the relationship in step (b), the Rs_{TOTAL}, and the desired Rs value (Rs target value) for said copper layer in each of the plurality of wafers.

19. (Original) The method of claim 13 wherein the oxide (Cu, or TaN) polish time is determined by using the equation:

$$PT_t = Rs_T - Rs_{TOTAL} / \alpha$$

where PT_t is the polish time for a particular wafer, Rs_T is the Rs target value provided for said copper layer, α is the polish rate in said oxide (Cu, or TaN) polish process, and Rs_{TOTAL} is the value from step (c).

20. (Original) The method of claim 19 further comprised of modifying the polish time in step (e) based on post oxide (Cu, or TaN) polish measurement data by including a disturbance factor (d_K) wherein the modified equation is the following:

$$PT_t = Rs_T - Rs_{TOTAL} / \alpha + d_K$$

where $d_K = (1 - \lambda)d_{K-1} + \lambda\,(Rs_T - Rs_{n,\,TOTAL} - \alpha\, PT_{K-1})$ in which d_{K-1} and PT_{K-1} indicate a disturbance factor and oxide (Cu, or TaN) polish time, respectively, for the (n-1)th wafer in the plurality of wafer, $Rs_{n,TOTAL}$ is Rs_{TOTAL} for the nth wafer in a said plurality of wafers, and λ is a numerical value between 0 and 1.

21. (Original) The method of claim 20 wherein d_{K-1} is equal to 0 for the first wafer in the plurality of wafers to be polished in the oxide (Cu, or TaN) polish process.

22. (Original) The method of claim 20 wherein said post oxide (Cu, or TaN) polish measurement data include the polish rate of said copper layer in said oxide (Cu, or TaN) polish step on at least one wafer that has been processed in the process tool.

23. (Original) The method of claim 20 wherein any filter algorithm may be used to update said d_{K-1}.

24. (Original) The method of claim 13 wherein said steps (b) – (e) are performed by a computer that is part of an advanced process control (APC) system which includes an APC controller that receives input from the computer and sends commands to one or more polish tools via a tool application program (TAP) and tool control system (TCS).

25. (Original) The method of claim 24 wherein the computer contains a feed forward (FF) model and a feed backward (FB) model wherein the FF model receives measurement data related to said sequence of processing steps and is used to perform steps (c) – (e) and wherein the FB model receives post oxide (Cu, or TaN) polish measurement data and is also used for step (e).

26. (Original) The method of claim 24 wherein said APC controller is linked to more than one CMP process tool and to more than one computer that provides data input.

27. (Withdrawn) An advanced process control (APC) system for controlling copper Rs in a polish process of a copper layer formed on a barrier layer within an opening in a dielectric layer on a wafer, said copper layer has a cross-sectional area and said wafer is one of a plurality of wafers having a copper layer to be polished, comprising:

(a) a computer having an APC feed forward (FF) model, an APC feed backward (FB) model, and an interface for user input, said FF and FB models are used to calculate a polish time and a copper thickness target for said copper layer on each of said plurality of wafers;

(b) an APC controller that is linked to said computer; and

(c) a polish process tool with a tool application program (TAP) and a tool control system (TCS) that is linked to the APC controller which forwards information to the TCS for each wafer to be polished and wherein the TCS is linked to said computer to provide post polish rate data.

28. (Withdrawn) The APC system of claim 27 wherein said feed forward (FF) model is activated by receiving metrology data relating to the cross-sectional area of said copper layer on each of said plurality of wafers and by receiving Rs target data for said copper layer to be polished.

29. (Withdrawn) The APC system of claim 27 wherein said FF model determines a copper thickness target for the copper layer to be polished on each of said plurality of wafers and wherein said copper thickness target value is inputted to said TCS via said APC controller prior to the polish process on each of said plurality of wafers.

30. (Withdrawn) The APC system of claim 27 wherein said copper thickness target is determined by a sequence comprising the following steps:

(a) determining a relationship between the cross-sectional area of said copper layer and Rs by plotting (1/cross-sectional area) vs. Rs results for a plurality of wafers;

(b) determining the total Rs (Rs_{TOTAL}) for the copper layer before said polish process; and

(c) obtaining an Rs target (Rs_T) value for the copper layer and adjusting Rs_T with the Rs_{TOTAL} value to give an adjusted Rs_T value that is inputted to the relationship in step (a) to determine the copper thickness target.

31. (Withdrawn) The APC system of claim 27 wherein said feed backward (FB) model is activated by inputting post polish removal rate data for a wafer from the TCS to said computer and wherein an adjusted copper polish rate for a subsequent wafer to be polished is inputted to said TCS via said APC controller from the computer.

32. (Withdrawn) The APC system of claim 30 wherein said FF model calculates the Rs total for the polish process by using the equation:

$$Rs_{TOTAL} = Rs_{PHOTO} + Rs_{CVD} + Rs_{ECP} + Rs_{ETCHING}$$

where Rs_{PHOTO}, Rs_{CVD}, Rs_{ECP}, and $Rs_{ETCHING}$ are terms that represent contributions from a patterning (photo) step, a CVD step, a copper deposition (ECP) step, and an etching step, respectively, to a variation in the width and thickness of said copper layer.

33. (Withdrawn) The APC system of claim 27 wherein the polish time for said polish process is determined in said FF model from the polish time equation:

$$PT_t = Rs_T - Rs_{TOTAL} / \alpha$$

where PT_t is the polish time for a particular wafer, Rs_T is the Rs target value, and α is the polish rate for a copper layer on a previously processed wafer in said polish process.

34. (Withdrawn) The APC system of claim 33 wherein the FB model modifies the polish time for a subsequent wafer to be polished by including a disturbance factor d_K to give an updated polish time equation:

$$PT_t = Rs_T - Rs_{TOTAL} / \alpha + d_K$$

where $d_K = (1 - \lambda)d_{K-1} + \lambda\,(Rs_T - Rs_{n,\,TOTAL} - \alpha\, PT_{K-1})$ in which d_{K-1} and PT_{K-1} indicate a disturbance factor and polish time, respectively, for the (n-1)th wafer in the plurality of wafers to be polished, $Rs_{n,\,TOTAL}$ for the nth wafer in a plurality of wafers to be polished, and λ is a numerical value between 0 and 1.

35. (Withdrawn) The APC system of claim 34 wherein d_{K-1} is equal to 0 for the first wafer in the plurality of wafers to be polished in said polish process.

36. (Withdrawn) The APC system of claim 34 wherein any filter algorithm may be used to update said d_{K-1}.

37. (Withdrawn) The APC system of claim 27 wherein said APC controller functions as a server and controls up to 20 polish process tools.

38. (Withdrawn) The APC system of claim 27 wherein the Rs 3σ variation for a polish process is reduced compared with an APC system for a polish process that includes only a feed backward model.

39. (Withdrawn) The APC system of claim 27 further comprised of an additional one or more links from post polish measurement tools that provide copper thickness data to said FB model.

40. (Withdrawn) The APC system of claim 27 wherein the polish process in an oxide (Cu, or TaN) polish that is performed in a CMP tool, said oxide (Cu, or TaN) polish process reduces the thickness of one or more of said copper layer, TaN layer, and dielectric layer.